CLAIMS

We claims:

1. A dry etching process for producing vertical sidewalls in X and Y crystalline directions along a compound semiconductor material comprising the steps of:

placing in a chamber said compound semiconductor material having an exposed portion;

releasing an halogen etchant into said chamber;

adding a nitrogen gas to said chamber;

heating said compound semiconductor material;

applying pressure to said halogen etchant and said nitrogen gas;

applying a bias power and a pulse-modulated power to said halogen etchant and said nitrogen gas; and

continuing the dry etching process until a desired via-hole is achieved.

2. A dry etching process as recited in Claim 1 wherein said compound semiconductor material has an etch rate that is within a range of approximately 70 times to approximately 80 times faster than said etch rate of a front-side metal layer on said compound semiconductor material.

3. A dry etching process as recited in Claim 1, wherein said chamber contains by volume not less than 10 parts halogen etchant to 1 part said nitrogen gas.

4. A dry etching process as recited in Claim 3, wherein said halogen etchant is one selected from the group consisting of Chlorine, Fluorine and Bromine.

5. A dry etching process as recited in Claim 3, wherein said halogen etchant is one selected from the group consisting of Hydrogen Bromide and Hydrogen Iodide.

6. A dry etching process as recited in Claim 1, wherein said halogen etchant is Hydrogen Bromide.

7. A dry etching process as recited in Claim 1, wherein said compound semiconductor material is selected from a group consisting of Gallium Arsenide and Indium Phosphide.

8. A dry etching process as recited in Claim 1, wherein said volume ratio of said halogen etchant to said nitrogen gas is selected from a range of approximately 10:1 to approximately 13:1.

9. A dry etching process as recited in Claim 1, wherein said heating step comprises applying a temperature to said halogen etchant and said nitrogen gas selected from a range of approximately 130 degrees C to approximately 170 degrees C.

10. A dry etching process as recited in Claim 1, wherein applied pressure of said halogen etchant and said nitrogen gas is selected from a range of approximately 5 milli-Torr to approximately 20 milli-Torr.

11. A dry etching process as recited in Claim 1, wherein said bias power step comprises introducing a bias power to said semiconductor material selected from a range of approximately 20 Watts to approximately 50 Watts.

12. A dry etching process as recited in Claim 1, wherein said pulse-modulated power step comprises applying an inductively coupled plasma power to said compound semiconductor material selected from a range of approximately 350 Watts to approximately 750 Watts.

13. A dry etching process as recited in Claim 1, wherein a non-exposed portion of said semiconductor wafer is not damaged during said etching process.

14. A dry etching process as recited in Claim 1, wherein said addition of said nitrogen gas to said halogen etchant reduces said etch rate of said front-side metal layer by more than 90 percent.

15. A dry etchant for a compound semiconductor material comprising:

a halogen etchant; and

a nitrogen gas, wherein a volume ratio of said halogen etchant to said nitrogen gas is greater than 10:1.

16. A dry etchant as recited in Claim 15, wherein said halogen etchant is selected from a group consisting of Chlorine, Fluorine, Bromine and Iodide.

17. A dry etching as recited in Claim 15, wherein said halogen-comprising compound is selected from a group consisting of Hydrogen Bromide, Hydrogen Iodide and Hydrogen Chloride.

18. A dry etching process for producing vertical sidewalls in X and Y crystalline directions for a compound semiconductor material comprising the steps of:

placing in a chamber said compound semiconductor material having an exposed portion;

releasing a halogen etchant into said chamber;

adding nitrogen gas to said chamber;

heating said compound semiconductor material;

applying a bias power and an inductively coupled plasma power to said halogen etchant and said nitrogen gas; and

continuing the dry etching process until the desired via-hole is achieved.

19. The method of Claim 18 wherein said dry etch process has an etch rate within a range of approximately 70 times to approximately 80 times faster than said etch rate of a front-side metal layer disposed said compound semiconductor material.

20. The method of claim 18 wherein said halogen etchant to said nitrogen gas volume ratio is selected from a range of approximately 10:1 to approximately 12:1.